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MAGNETOSTATIC WAVE TECHNOLOGY

Massachusetts Institute of Technology

A.R. Calawa, R.A. Murphy

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Rome Laboratory
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APPROVED: Peter J. Rainville

PETER J. RAINVILLE
Project Engineer

FOR THE COMMANDER: John K. Schindler

JOHN K. SCHINDLER, Director
Electromagnetics & Reliability Directorate

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A. R. Calawa, R. A. Murphy

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Massachusetts Institute of Technology
P O Box 73
Lexington MA 02173-9108

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13. ABSTRACT (Maximum 200 words)

The integration of GaAs with ferrimagnetic garnets was investigated and demonstrated. A hybrid technique was first used to integrate two GaAs circuits with yttrium-iron garnet (YIG) delay lines, demonstrating the feasibility and benefits of combining the two materials in special microwave operations. The epitaxial growth of single-crystal GaAs on gadolinium-gallium garnet (GGG) was then accomplished, demonstrating a first step in the monolithic integration of the two materials. The hybrid circuit, consisting of a GaAs microwave circuit integrated with a tapped YIG delay line, formed an oscillator with an extremely short external delay loop, and taps provided multiple outputs with long delay times. The oscillator was tunable from 2.76 to 2.95 GHz with a 3-dB bandwidth of 10kHz. The first growth of GaAs on GGG was sucessfully performed by using an InAs buffer layer and an InAs/GaAs multilayer structure between the GGG and the GaAs. The unintentionally doped InAs layers were n-type with room-temperature donor concentrations in the range of 7×10^{16} to 2×10^{18} cm^{-3}, and corresponding mobilities were 3.5×10^{3} to 1×10^{3} cm^{2}/V s. Hall measurements indicated that the GaAs was conducting. These were the first electrical measurements ever reported for any III-V compound semiconductor deposited on a garnet.

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ABSTRACT

In this development, the integration of GaAs with ferrimagnetic garnets was investigated and demonstrated. A hybrid technique was first used to integrate two GaAs circuits with yttrium-iron garnet (YIG) delay lines, demonstrating the feasibility and benefits of combining the two materials in special microwave operations. The epitaxial growth of single-crystal GaAs on gadolinium-gallium garnet (GGG) was then accomplished, demonstrating a first step in the monolithic integration of the two materials. These results were reported in three separate publications.

The first hybrid circuit demonstrated was a single-mode magnetostatic surface-wave delay-line oscillator that could be tuned continuously from 4.82 to 6.93 GHz without frequency jumping and without the need for a directional coupler. The circuit delivered an output power of 4.4 dBm at 6.1 GHz with a phase noise of -100 dBc/Hz at 10 kHz away from the oscillation frequency. The second hybrid circuit consisted of a GaAs microwave circuit integrated with a tapped YIG delay line. This integrated circuit formed an oscillator with an extremely short external delay loop, and taps provided multiple outputs with long delay times. The oscillator was tunable from 2.76 to 2.95 GHz with a 3-dB bandwidth of 10 kHz.

Finally, the first growth of GaAs on GGG was successfully performed by using an InAs buffer layer and an InAs/GaAs multilayer structure between the GGG and the GaAs. The unintentionally doped InAs layers were n-type with room-temperature donor concentrations in the range of 7×10^{16} to 2×10^{18} cm^{-3}, and corresponding mobilities

were 3.5×10^3 to 1×10^3 cm^2/V s. Hall measurements indicated that the GaAs was conducting. These were the first electrical measurements ever reported for any III-V compound semiconductor deposited on a garnet.

1. INTRODUCTION

In most microwave-circuit applications, microwave signals must be identified, isolated, controlled, and processed. To perform these functions, low-loss passive devices such as delay lines, filters, resonators, correlators, convolvers, and circulators are required. Surface acoustic wave (SAW) devices have been used to perform most of these functions, but their operation is limited to frequencies in the megahertz range. This necessitates the conversion of signals at microwave frequencies to SAW frequencies for processing and then, in some instances, back to microwave frequencies.

For the past ten years, the use of magnetostatic waves (MSWs) in ferrimagnetic garnets has been investigated to perform these functions at microwave frequencies. Several MSW components, such as delay lines, filters, resonators, correlators, and convolvers, have been realized and used for analog-signal identification, control, and processing.[1] These components enable a substantial reduction in the device size required for long delays, because MSWs travel with velocities two to four orders of magnitude slower than electromagnetic waves. In addition, ferrimagnetic garnets are widely used in isolators and circulators to provide isolation in appropriate parts of a microwave circuit. Ferrimagnetic circulators can operate from 0.5 to 26.5 GHz and have wide bandwidths and low insertion losses.[2]

The monolithic integration of semiconductors with devices based on ferrimagnetic materials would represent a significant advance in microwave-circuit technology. Such a capability would, for example, enable ferrimagnetic circulators to be monolithically incorporated in phased-array radar modules, resulting in significant reductions in size and weight. The primary factor limiting this capability is the difficult materials challenge of growing high-quality semiconductor films, such as GaAs, on ferrimagnetic substrates. The ferrimagnetic materials are garnets, which have a cubic crystal lattice like most of the

widely used semiconductors but have a lattice parameter which is more than twice that of GaAs.

Because of its low propagation loss, the most frequently used ferrimagnetic film is yttrium-iron garnet (YIG) grown by liquid phase epitaxy on a gadolinium-gallium garnet (GGG) substrate.[2] The GGG substrate is particularly desirable because it provides a lattice match to YIG films and allows essentially defect-free (< 1 defect/cm^2) films to be grown on large-diameter (> 3 in.) GGG wafers. The integration of magnetic microwave nonreciprocal devices and MSW devices with monolithic microwave integrated circuits (MMICs) is currently performed by hybrid techniques. One method used in this integration involves gluing or soldering the circuit chips and YIG devices together in order to make the wire interconnects. The objective of the initial phase of this program was to design circuits using this hybrid approach. This is a cumbersome process with a low yield, and the interconnect wires can limit the circuit performance. In the second phase of the program, the monolithic integration of semiconductor microwave devices with the nonreciprocal MSW devices was investigated in order to overcome these limitations. Molecular beam epitaxy (MBE) was used to grow GaAs on GGG, the first step in such an integration.

2. HYBRID INTEGRATION OF GaAs CIRCUITS WITH YIG

Two circuits were designed and built that demonstrate the utility of integrating active electronic devices with YIG delay lines. The material used was a 20-μm-thick layer of (111)-oriented YIG grown on a (111)-oriented GGG substrate by liquid phase epitaxy. The GaAs circuit was fabricated on an MBE-grown epitaxial layer. After dicing the circuit chip from the GaAs wafer, both the delay line and the microwave circuit chip were glued into a microwave package. Wire interconnects were used between the GaAs circuit and the YIG delay line. Details of the design and operation of these two circuits were published,[3,4] and the reports are provided here in Appendices A and B.

3. EPITAXIAL GROWTH OF GaAs on GGG

To our knowledge, there were only two previous reports of the epitaxial growth of III-V compounds on a garnet and both utilized organometallic vapor phase epitaxy. In one case,[5] an InP layer that contained several InGaAs quantum wells was grown on GGG. The lattice-constant mismatch between the InP and GGG was 52.6%. In the second case,[6] a GaAs film was grown on a garnet in which the rare earth composition was adjusted to obtain lattice sites that were more nearly coincident with the GaAs lattice sites. The mismatch was 52.7%. Electrical characterization of the layers was not reported in either case.

In this program, we investigated the use of MBE to grow GaAs on GGG, which is, as mentioned above, a commonly used substrate for the deposition of ferrimagnetic films.[7] We developed a technique in which an initial layer of single-crystal InAs is first grown on a GGG substrate. Single-crystal layers of InAs can be grown on GGG because the lattice constant of InAs is nearly one half that of GGG, enabling every other lattice site of the InAs layer to coincide with the GGG lattice sites. We then grew a carefully graded superlattice of InAs and GaAs on the InAs layer to make the transition to GaAs while maintaining the semiconductor crystallinity.

Although the initial structures that were grown were crystalline, they could not be electrically characterized because both the GaAs and InAs were conductive, making it impossible to differentiate between the conductivity of the two materials. In work performed subsequent to the completion of this program, low-temperature-grown (LTG) GaAs was utilized to isolate the uppermost layer of GaAs from the layers below.[8] At present, the active GaAs layer appears to be compensated by a factor of about 2.4, having a carrier concentration of 8×10^{16} cm^{-3} when the intended concentration was 2×10^{17} cm^{-3}.

Also, the surface morphology of the GaAs was not adequate for device processing, a problem which remains.

Prior to achieving the above results, an extensive investigation of methods for cleaning the surface of YIG or GGG prior to growth and of the MBE growth parameters required to grow GaAs on YIG or GGG was undertaken. It would be most desirable to grow GaAs on a (111) crystallographic plane of YIG or GGG because this is the orientation on which the magnetic garnets are grown and are commercially available. Consequently, most of the early investigations were attempts to grow the GaAs directly on (111)-oriented YIG films and GGG substrates. Although these attempts proved unsuccessful, we have included a description of these experiments in this report to make the reader aware of the pitfalls in this technology and to describe the chemical reactions that can inhibit epitaxial growth.

4. EXPERIMENTAL APPARATUS

A Varian GEN II MBE system was used to perform all the epitaxial growths. Our MBE system has a base pressure of 10^{-10} Torr and is only used to grow As-based semiconductor compounds. The system is equipped with a reflection high-energy electron-diffraction (RHEED) apparatus, which we use regularly to determine substrate temperature, growth rate, and the crystalline quality of a growing surface. The ability to monitor the surface-lattice construction during growth provides an extremely powerful tool for the study of the heteroepitaxial growth of lattice-mismatched crystals. We have learned, however, that if chemical reactions occur between the incident vapor species and the substrate, the RHEED diffraction patterns can be misleading. In addition to RHEED, we have used x-ray diffraction, Auger electron spectroscopy, Hall measurements, Nomarski microscope observations, and scanning electron microscopy (SEM) to characterize the epitaxial layers.

A schematic diagram of the RHEED apparatus is shown in Fig. 1, together with three characteristic RHEED patterns. An electron beam, which can be varied in energy from 0 to 20 KeV, impinges on the growing surface at a grazing angle of only a few degrees, is diffracted from the surface, and activates a fluorescent screen. The component of electron energy normal to the surface is only a few hundred electron volts, so that the diffracted electron beam only samples about three monolayers of the crystal surface. The streaked lower-diffraction pattern of Fig. 1 simulates a pattern of lines emerging from a surface that is both crystalline and extremely flat within the impinging beam area. The spotted center-diffraction pattern of Fig. 1 is three-dimensional, caused by the diffraction of high-energy electron transmission through surface asperities. The observation of this pattern is a clear indication that the growing surface is becoming rough, probably because of three-dimensional growth. If the spots remain sharp and well defined, the growth must be crystalline. The Debye-Scherrer rings shown in the top diffraction pattern of Fig. 1 are a clear indication of polycrystalline growth. If no diffraction pattern is seen on the RHEED screen, then the growing layer is very likely amorphous. The physical spacings between the diffraction streaks or spots are inversely related to lattice spacing of the surface atoms. These spacings may differ from those obtained from a bulk lattice because of the chemical arrangement of dangling bonds from surface atoms, which form in the way that minimizes surface energy. Thus, much can be learned about the growing surface while the growth is taking place. Furthermore, if the substrate crystal is more stable and has a significantly lower vapor pressure than the epilayer, the layer that is grown can be thermally reevaporated from the substrate and the growth may be reinstated with different growth parameters. This was the case for the growth of GaAs on GGG. However, the technique was not used in this research because of concern that a chemical reaction with the GGG could cause the reevaporation of an undesirable species (like oxygen) into our heavily utilized MBE system.

5. EXPERIMENT

5.1. GROWTH ON (111)-ORIENTED YIG

The chemical composition of GGG is $Gd_3Ga_5O_{12}$, and the basic crystal structure is cubic with a lattice parameter of 12.383 Å. The basic crystal structure of GaAs is also cubic, but the lattice parameter is only 5.653 Å. The lattice-constant mismatch between the two structures is thus 53.4%. Even if the GaAs were to be grown such that every second GaAs site were coincident with a GGG site, the mismatch would be 8.7%. In spite of this large mismatch, numerous attempts were made to grow GaAs directly on (111)-oriented YIG by MBE using a variety of MBE growth conditions and techniques. These experiments are described by Tables I through VIII. As previously stated, none of these experiments were successful, but they are described here to provide guidance to other workers in this area.

Since the (111)-oriented YIG was in the form of a 20-μm-thick epilayer grown on a (111)-oriented GGG substrate by liquid phase epitaxy, no mechanical polishing was used in these experiments. Instead, both chemical and thermal etching procedures were employed. The surface treatments of the YIG substrates are given in column 5 of Tables I through VIII. With the exception of growth-run numbers 3-1191 and 3-1201, all substrates were degreased and etched prior to mounting in the MBE system. The degreasing procedure consisted of 10-min boil in a 1:1:1 solution of trichloroethane, acetone, and methanol, followed by a room-temperature rinse in acetone and methanol and drying in a stream of dry nitrogen. Etching consisted of immersing the substrate in a 1:1 solution of phosphoric and sulfuric acid heated to 150°C, followed by a 5-min rinse in deionized (DI) water. This etch removed less than 0.1 μm of the YIG.

In all cases, the substrates were mounted on a Mo substrate holder with In solder and placed in the preparation chamber of the MBE system. All thermal treatments were done in the MBE system. Most of the heat treatments were done in the preparation chamber with

the exception of those in which an As flux was used or where the growth was interrupted to heat treat the sample. These were done in the growth chamber.

In Tables I through VIII, the RHEED pattern observed is given by column 6, and a one-word qualitative description of the result of the growth experiment is given in column 7. Results described as poly means that the epilayer is polycrystalline as determined by the RHEED pattern and as substantiated by x-ray rocking curves when the layers were thick enough. A rough layer refers to the surface morphology of the layer as observed in the Nomarski microscope. A no epi result is an epilayer growth where no change in the RHEED pattern was observed. This either meant that the Ga and As reevaporated from the YIG surface at the high substrate temperature or that a foreign film was formed by chemical reaction with the YIG, which could be removed with buffered hydrofluoric acid.

As Table I indicates, growths performed at the normal growth temperature of 580°C were polycrystalline. Different nucleation procedures were used in the process of these investigations, which are also included in column 5 under surface treatment. Note, for example, in growth-run number 3-1191, the substrate was exposed to an As flux for 10 min while at 200°C followed by a second 10-min As exposure at 400°C. The second exposure was used because no change was observed in the RHEED pattern after the first exposure. Apparently neither exposure had any effect on the substrate. After the second exposure, 200 Å of GaAs was grown at the very slow rate of 0.1 μm/h. At this point the RHEED pattern deteriorated, indicating the onset of polycrystalline growth. Subsequent attempts to obtain crystalline growth at higher temperatures failed. This pattern was generally true for all growths. If the initial growth was polycrystalline, a crystalline structure could not be obtained either by annealing or by subsequent growth at a different temperature.

When growth temperatures above ~ 650°C were used, as described by Table II, the RHEED patterns indicated that the films grown were crystalline. However, the spacing

between the RHEED streaks did not change during the growth, which was indicative of no growth at all. When the surfaces of these layers were examined with an optical microscope, it was clear that change had indeed occurred as a result of the growth process, and in fact a thin film was observed. However, these thin crystalline films were always highly insulating and could easily be etched from the substrate with hydrofluoric acid. We concluded that the films were not GaAs but an oxide formed by a chemical interaction with the YIG film. As Table III indicates, attempts to prevent this interaction by initiating GaAs growth at lower substrate temperature always produced polycrystalline films.

A number of different buffer layers were used in an attempt to properly initiate growth. As Table IV describes, GaAs/InGaAs superlattices, an annealed GaAs layer, and a LTG GaAs layer were evaluated. Our experiments did not yield crystalline growth for any of these buffer layers.

Table V shows the results of experiments in which higher growth rates were used. In several cases, dendritic growth was observed. An example of such dendritic growth as observed by a SEM is shown in Fig. 2. Table VI shows the results of experiments in which the growth was interrupted at various points in the growth process in an attempt to stabilize the growing surface. Generally, rough or polycrystalline surfaces were obtained.

Table VII shows the results of evaluations of the growth of $Al_{0.3}Ga_{0.7}As$ and $In_{0.5}Ga_{0.5}As$ on YIG. Rough films were produced. Table VIII shows the results of using Ga or Al layers to initiate growth. Either no growth or rough epi was observed.

From these experiments we concluded that GaAs could not be grown on (111)-oriented YIG by MBE, and that because of the nearly identical crystal structures of YIG and GGG, MBE-grown GaAs also could not be deposited epitaxially on (111)-oriented GGG. Since previous successful epitaxial growths of III/V semiconductors were all obtained on (100)-oriented garnet substrates, we purchased a large GGG ingot from which substrates with different orientations could be cut.

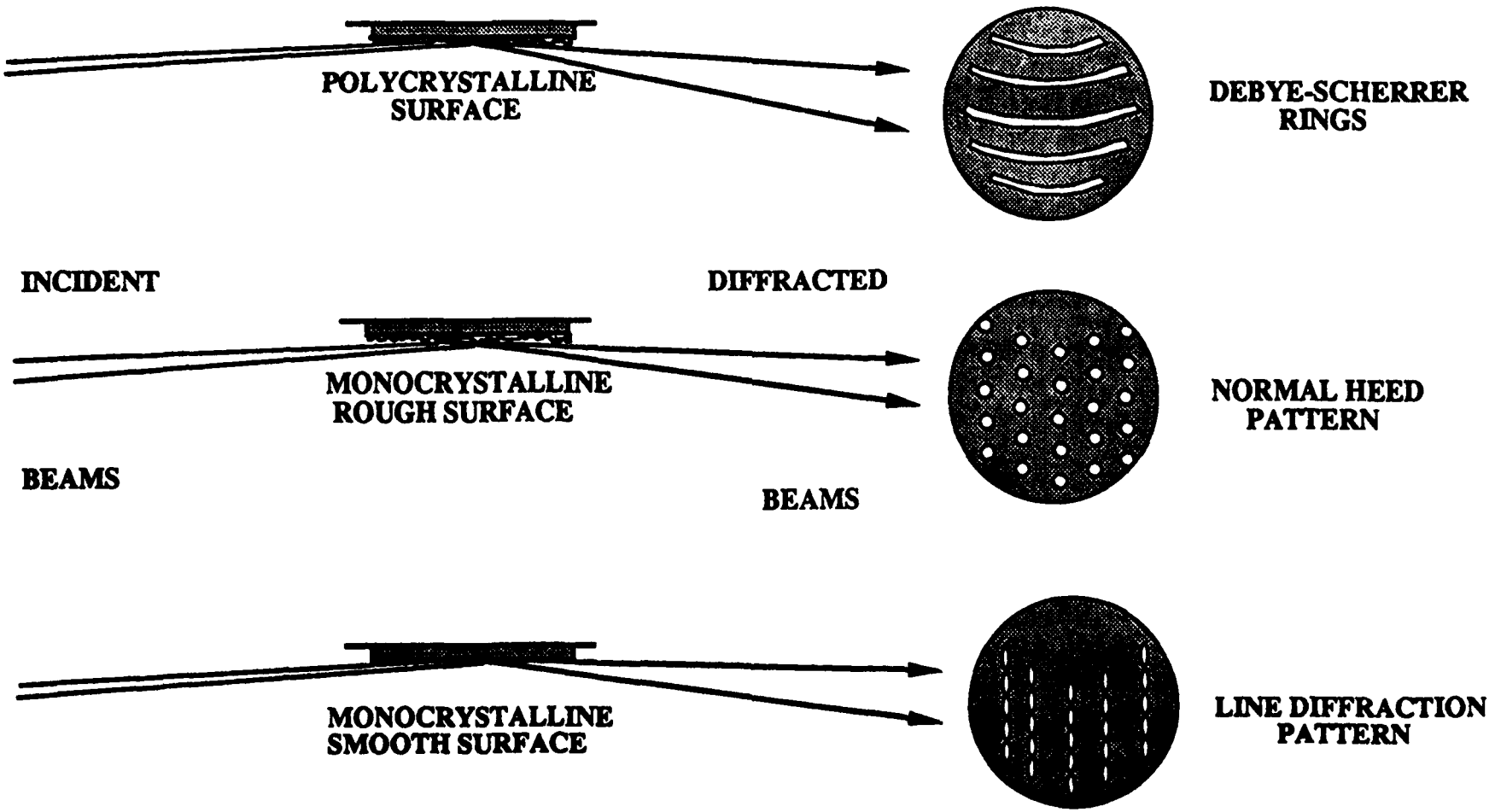

Fig. 1 Schematic representationn of RHEED patterns obtained with three different surfaces.

Fig. 2. SEM micrograph showing dendritic growth of GaAs on YIG.

5.2. GROWTH ON (100)-ORIENTED GGG

Tables IX and X describe our first attempts to grow GaAs directly on (100)-oriented GGG, with Table X summarizing experiments in which we attempted to dope the films using Si. Here again we were not able to obtain single-crystal GaAs or produce measurable conductivity in the films. However, for nearly all of the growths, the final RHEED patterns were either rings, spots, or a combination of the two. Since it is known that a rough crystalline surface will result in a spotted RHEED pattern, we obtained x-ray rocking curves from all layers with spot patterns. The x-ray rocking curves showed a clear dominance of (111) GaAs although several other peaks were also observed. The tendency toward (111) GaAs growth led us to believe that given a slight decrease in the lattice mismatch between the GaAs and GGG it should be possible to grow crystalline layers.

It was clear that a buffer material was required between the GGG and the GaAs. A suitable material would provide a better match of coincident lattice sites and would be grown at a lower substrate temperature to prevent any possible chemical reaction with the GGG. The material chosen for this layer was InAs.

The lattice parameter of InAs is 6.059 Å, and the crystal structure is the same as that of GaAs. Thus, the lattice-constant mismatch between every second InAs site to the GGG sites is only 2.1%. Moreover, the MBE temperatures used for depositing InAs are generally lower, so it was plausible that growth could be initiated at a sufficiently low temperature to prevent chemical interaction with the GGG. An InAs/GaAs strained-layer superlattice could then be used to accommodate some of the strain existing in the GaAs due to the GaAs/InAs lattice mismatch.

Table XI summarizes the growths of InAs on (100)-oriented GGG. A new surface cleaning step was included at this time, which consisted of heating the GGG substrate in the growth chamber to 600°C while exposing it to an In flux of 2×10^{14} atoms/cm^2 for 10 min. Since both the In and its oxides are volatile at this temperature, they will reevaporate and cleanse the surface of any loosely bound oxygen. The nucleation step for

each layer consisted of the growth of 30 Å of InAs at a substrate temperature of 300°C. X-ray rocking curves were obtained for each of these layers and all were found to be crystalline. Since we have had considerable experience growing pseudomorphic InGaAs on GaAs, it was reasonable to assume that we would be able to grow GaAs on the InAs if we grew a multilayer structure where each subsequent layer of InGaAs would have a higher Ga concentration and a layer thickness that was slightly less than the pseudomorphic limit for single-crystal growth on the preceding layer. The layers that were grown to achieve this goal are described by Table XII. As indicated by the last growth sequence in the table, we succeeded in growing a 1-μm-thick layer of GaAs on an InAs/GaAs superlattice. We have since successfully repeated this growth procedure and have again obtained single-crystal GaAs. Details of the procedure used to grow single-crystal GaAs on GGG were published,[9] and the report is provided here in Appendix C.

6. FUTURE APPLICATIONS

Although the cost and size of GaAs active components has been substantially reduced by monolithic technology developed in a number of programs, the monolithic integration of magnetic components, such as circulators, isolators, and filters, has largely not been addressed. The technology that has been developed in this program offers the capability of fabricating monolithic components that incorporate nonreciprocal magnetic materials and active GaAs solid-state devices. An example of such a component is a magnetic YIG filter with an integral GaAs field-effect transistor amplifier. In any case, the next step in the development of this area is to identify the best application for this new materials technology and demonstrate it in a useful magnetic component.

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TABLE I

GROWTH OF GaAs ON (111)-ORIENTED YIG UNDER NORMAL GaAs GROWTH CONDITIONS

RUN NO.	GROWTH TEMP. (°C)	GROWTH TIME (min)	GROWTH RATE (μm/h)	SURFACE TREATMENT	RHEED PATTERN	RESULTS
3-1191				1000°C-1 h	streaks	
				850°C-10 min	streaks	
				200°C/As-10 min	streaks	
				400°C/As-10 min	streaks	
	200		0.1	200 Å GaAs	faint rings	
	630	10	0.1	GaAs	rings	
	580	25	1.0	GaAs	rings	poly
3-1201				800°C-10 min	streaks	
				350°C/As	streaks	
				400-580°C/As	streaks	
	580	30	1.0	GaAs	rings	poly

TABLE II

GROWTH OF GaAs ON (111)-ORIENTED YIG USING HIGHER GROWTH TEMPERATURE

RUN NO.	GROWTH TEMP. (°C)	GROWTH TIME (min)	GROWTH RATE (μm/h)	SURFACE TREATMENT	RHEED PATTERN	RESULTS
3-1267				degrease, etch		
				850°C-1 min	streaks	
	650	12	0.1	GaAs	streaks	no epi
3-1268				degrease, etch		
				5 min DI water	streaks	
	650	12	0.1	GaAs	streaks	no epi
3-1332				degrease, etch		
	680	5	1	GaAs	streaks	
	680	78	1	GaAs	rings	
				anneal 600°C	streaks	high ohms no epi
3-1357				degrease, etch		
	680	5	1	GaAs	streaks	
	680	225	1	GaAs	rings	poly

TABLE III

GROWTH OF GaAs ON (111)-ORIENTED YIG USING LOWER GROWTH TEMPERATURE

RUN NO.	GROWTH TEMP. (°C)	GROWTH TIME (min)	GROWTH RATE (μm/h)	SURFACE TREATMENT	RHEED PATTERN	RESULTS
3-1269	550	12	0.1	degrease, etch start run end run	 streaks faint spots	 rough
3-1270	500	12	0.1	degrease, etch 600°C-10 min start run end run	 streaks streaks rings	 poly
3-1271	550	12	0.1	degrease, etch 650°C-10 min GaAs at start run GaAs at end run	 streaks streaks faint spots	 rough

TABLE IV

GROWTH OF GaAs ON (111)-ORIENTED YIG USING VARIOUS BUFFER LAYERS

RUN NO.	GROWTH TEMP. (°C)	GROWTH TIME (min)	GROWTH RATE (μm/h)	SURFACE TREATMENT	RHEED PATTERN	RESULTS
3-1274				degrease, etch		
	550		1	GaAs/InGaAs-SL*		
				50 Å/50 Å-10 periods	streaks	
	550	10	1	GaAs	streaks	
	550	30	1	GaAs	rings	poly
3-1285				Preclean		
	550		0.1	GaAs/InGaAs-SL	streaks	
				50 Å/50 Å-10 periods	streaks	
	550	960	0.1	after 5000 Å GaAs	faint rings	
				end run	rings	poly
3-1289				degrease, etch		
	550		0.1	200 Å GaAs	streaks	
			1	GaAs/InGaAs-SL		
	550	20	1	GaAs	rings	poly
3-1294				degrease, etch		
	600		0.1	200 Å GaAs		
				anneal 600°C-1 h	streaks/spots	
	600	240	0.1	GaAs	spots	dendrites
3-1351				degrease, etch		
	680	5	1	GaAs	streaks	
	680	6	1	GaAs	streaks	
	550	5	1	GaAs	rings	
	200	120	1	LTG GaAs	rings	
	680	30	1	GaAs	rings	poly

*Superlattice.

TABLE V

GROWTH OF GaAs ON (111)-ORIENTED YIG USING HIGHER GROWTH RATES

RUN NO.	GROWTH TEMP. (°C)	GROWTH TIME (min)	GROWTH RATE (μm/h)	SURFACE TREATMENT	RHEED PATTERN	RESULTS
3-1307				degrease, etch		
	600	0.5	0.3	GaAs	faint	
	600	42	0.3	GaAs	spots	dendrites
3-1308				degrease, etch		
	600	0.5	0.5	GaAs	faint streaks	
	600	60	0.5	GaAs	spots	dendrites
3-1310				degrease, etch		
	600	10		GaAs		
	600	120	0.5	GaAs	rings	
				anneal/no As	streaks	no epi

TABLE VI

GROWTH OF GaAs ON (111)-ORIENTED YIG USING INTERRUPTED GROWTH

RUN NO.	GROWTH TEMP. (°C)	GROWTH TIME (min)	GROWTH RATE (μm/h)	SURFACE TREATMENT	RHEED PATTERN	RESULTS
3-1312				degrease, etch		
	600	10	1	GaAs	streaks	
	600	120	1	GaAs interrupt- 6 min on/ 1 min off		
				GaAs	ring	
	600	1		anneal/no As	rings	no PL,* rough
3-1315				degrease, etch		
	600	10	1	GaAs	streaks	
	600	240	1	GaAs interrupt- 1 min on/ 1 min off		
				8 cycles	no rings	
				20cycles-on/	rings	
				off	*no rings*	
				60 cycles-on/	rings	
				off	no rings	
				82 cycles-on/	rings	
				off	rings	
				135 cycles-on/	rings	
				off	rings	
				anneal-5 min	rings	
				anneal-1 h	rings	rough
3-1322				degrease, etch		
	650	50	1	GaAs	streaks	
	620	3	1	GaAs	streaks	
				620°C anneal- 2 min	streaks	
	630	3	1	GaAs	streaks	
				620°C anneal- 2 min	streaks	
	640		1	3 min on/ 2 min off	rings	poly

*Photoluminescence.

TABLE VII

GROWTH OF $Al_{0.3}Ga_{0.7}As$ AND $In_{0.5}Ga_{0.5}As$ ON (111)-ORIENTED YIG

RUN NO.	GROWTH TEMP. (°C)	GROWTH TIME (min)	GROWTH RATE (μm/h)	SURFACE TREATMENT	RHEED PATTERN	RESULTS
3-1323				degrease, etch		
	680	7	1	GaAs	streaks	
	680	120		GaAs	streaks	
	680	0.25	1	$Al_{0.3}Ga_{0.7}As$	none	rough
3-1324				degrease, etch		
	680	5		GaAs	streaks	
	680	5	1	GaAs	streaks	
	680	0.1	1	$Al_{0.3}Ga_{0.7}As$	faint	
				end run	none	rough
3-1326				degrease, etch		
	680	5	1	GaAs	streaks	
	680	0.1	1	$Al_{0.3}Ga_{0.7}As$	faint	
	680	5	1	GaAs	none	rough
3-1343				degrease, etch		
	680	5	1	GaAs	streaks	
	550	6	1	$In_{0.5}Ga_{0.5}As$	none	rough

TABLE VIII

GROWTH OF GaAs ON (111)-ORIENTED YIG USING INITIAL Ga OR Al LAYERS

RUN NO.	GROWTH TEMP. (°C)	GROWTH TIME (min)	GROWTH RATE (μm/h)	SURFACE TREATMENT	RHEED PATTERN	RESULTS
3-1336				degrease, etch		
	680	5	1	GaAs	streaks	
				Ga-3 s/no As	faint	
	680	120	1	GaAs	rings	
				anneal-600°C/ no As	streaks	no epi
3-1337				degrease, etch		
	680	5	1	GaAs	streaks	
				Ga-3 s/no As	faint	
	680	25	1	GaAs	rings	
3-1342				degrease, etch		
	680	5	1	GaAs	streaks	
				Al-3 s/no As	faint	
	680	2	1	GaAs		
	680	25	1	GaAs	rings	rough

TABLE IX

GROWTH OF GaAs ON (100)-ORIENTED GGG

RUN NO.	GROWTH TEMP. (°C)	GROWTH TIME (min)	GROWTH RATE (μm/h)	SURFACE TREATMENT	RHEED PATTERN	RESULTS
3-1368				degrease, etch		
	680	5		GaAs	streaks	
	680	50	1	GaAs	streaks	
				end run	streaks	rough
3-1378				degrease, etch		
	680	5	1	GaAs	streaks	
	590	105	1	end run	spots/rings	poly
3-1381				degrease, etch		
				700°C-5 min/As	streaks	
				800°C-5 min/As	streaks	
				800°C-2 s/Ga	streaks	
	580	1	1	GaAs	rings	
				700°C/As	spots/rings	
	675	2	1	GaAs		
	650	2	1	GaAs	rings/spots	
	650	120			spots/lines	
					rings/spots	poly
3-1383				degrease, etch		
				700°C-5min/As	streaks	
	400	60	1	GaAs	rings	
	600	240	1	GaAs	spots/rings	
				end run	spots/lines	rough
3-1387				degrease, etch		
				700°C-5 min/As	streaks	
				200°C-20 min/As	lines	
	400	60	1	GaAs	rings	
	580	132	1	GaAs	rings	
				end run	rings	rough

TABLE X

DOPED GROWTH OF GaAs ON (100)-ORIENTED GGG

RUN NO.	GROWTH TEMP. (°C)	GROWTH TIME (min)	GROWTH RATE (μm/h)	SURFACE TREATMENT	RHEED PATTERN	RESULTS
3-1438				degrease, etch 5 min DI water	streaks	
	600	150	1	GaAs	rings	insulating
3-1439				degrease, etch 700°C-5 min/As	streaks	
				200°C-15 min/As	lines	
	580	240	1	after 1 h	spots/rings	
				end run	spots/rings	insulating
3-1450				degrease, etch 650°C-5 min/As	streaks	
	600	60	0.1	GaAs	lines	
	600	660	0.3	GaAs after 10 min	spots	
				end run	spots/rings	poly
3-1456	600	30	0.3	GaAs	rings/spots	
				600°C-2 h/As	rings/spots	poly

TABLE XI

GROWTH OF InAs ON (100)-ORIENTED GGG

GROWTH TEMP. (°C)	LAYER THICKNESS (Å)	RHEED PATTERN	CARRIER CONCENTRATION (cm^{-3})		CARRIER MOBILITY ($cm^2/V\ s$)	
			300 K	77 K	300 K	77 K
300 450	30 10,000	faint spots/rings	1.4×10^{17}	1.4×10^{17}	2376	2441
300 400	30 10,000	faint lines/spots	3.6×10^{17}	2.9×10^{17}	1337	1453
300 350	30 10,000	faint lines/spots	6.8×10^{17}	6.0×10^{17}	997	1079
300 350 400 500	30 7500 2500 5000	faint lines/rings faint lines	4×10^{17}	3.7×10^{17}	2034	2182
300 350 425 500	30 2500 2500 20,000	faint lines/rings lines	3.7×10^{17}	3.5×10^{17}	1317	1375
300 500	30 30,000	faint none visible	6.5×10^{16}	6.9×10^{16}	2966	2893

TABLE XII

GROWTH OF SINGLE-CRYSTAL GaAs ON (100)-ORIENTED GGG USING SUPERLATTICE

GROWTH TEMP (°C)	LAYER TYPE	LAYER THICKNESS (μm)	RHEED PATTERN	CARRIER CONCENTRATION (cm^{-3})		CARRIER MOBILITY ($cm^2/V\ s$)	
				300 K	77 K	300 K	77 K
300	InAs	1.25	rings/spots	1.8×10^{18}	1.2×10^{18}	913	958
325	InAs	1.0	lines/rings	1.0×10^{18}	9.7×10^{17}	1066	1112
400	InAs	1.2	sharp lines	6.9×10^{17}	6.5×10^{17}	1286	1309
450	InAs	1.0	lines/spots	4.0×10^{17}	3.9×10^{17}	1797	1834
400	InAs	1.0	sharp lines				
400	InAs	2.0	sharp lines				
400	50 Å InAs/ 50 Å GaAs superlattice	0.5	lines	no Hall data			
580	GaAs	1.0	lines	x-ray shows single-crystal InAs and GaAs			

APPENDIX A

Tunable Magnetostatic-Wave Oscillator Employing a Single GaAs MMIC Chip

C.L. Chen and L.J. Mahoney, Electronics Letters 25, 196 (1989)

This paper describes the hybrid integration of a single GaAs monolithic amplifier with a YIG delay line. The circuit is that of a single-mode magnetostatic surface-wave delay-line oscillator that can be tuned continuously from 4.82 to 6.39 GHz without frequency jumping and without the requirement of a directional coupler. The circuit delivered an output power of 4.4 dBm at 6.1 GHz with a phase noise of -100 dBc/Hz at 10 kHz away from the oscillation frequency.

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TUNABLE MAGNETOSTATIC-WAVE OSCILLATOR EMPLOYING A SINGLE GaAs MMIC CHIP

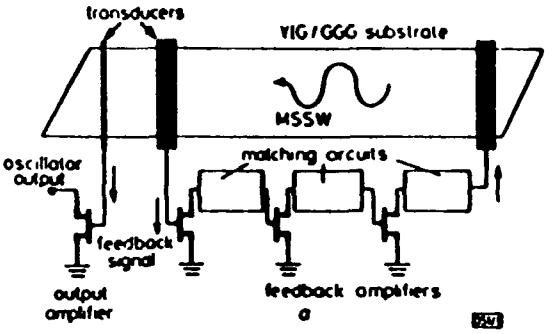
Indexing terms: Microwaves devices and components, Microwave oscillators, Magnetostatic waves, Integrated circuits

A microwave tunable magnetostatic surface-wave delay-line oscillator which employs a single GaAs monolithic amplifier chip in the feedback loop has been developed. No directional coupler is needed, and a single-mode oscillation can be tuned continuously from 4·82 to 6·39 GHz without frequency jumping. At 6·1 GHz, an output power of 4·4 dBm was measured with a phase noise of −100 dBc/Hz at 10 kHz offset from the oscillation frequency.

Introduction: Magnetostatic surface-wave (MSSW) delay lines have been used in microwave tunable oscillators.[1,2] The use of external amplifiers and directional couplers in these oscillators results in physically large components with long external electrical delays that cause frequent frequency jumping during tuning. We have previously reported on an MSSW delay-line oscillator, using multiple GaAs monolithic-microwave-integrated-circuit (MMIC) chips, which avoids the use of an external directional coupler in the feedback loop.[3] This design utilised planar technology in both the MSSW devices and the GaAs MMICs. However, this oscillator had narrow tunable range and multimode oscillation. This letter describes a new MSSW oscillator using a single GaAs monolithic amplifier chip which displays single-mode oscillation over a wide frequency range.

Oscillator design and fabrication: Fig. 1 shows the schematic diagram of the oscillator and a photograph of the GaAs chip. The GaAs circuit consists of a three-stage amplifier which provides the gain needed in the feedback loop. The output and the input of the amplifier are connected to four-finger narrowband transducers for the MSSW delay line. These multiple-finger transducers are used in order to realise single-mode oscillation. Each finger is 2 mm long and 25 μm wide with 25 μm spacings between fingers; the distance between the narrowband transducers is 2·5 mm. The oscillator signal is coupled to the gate of an output MESFET with a single-finger transducer and the output is obtained from the drain of this MESFET. This single-finger transducer is 50 μm wide and is positioned at 1 mm from the narrowband transducer of the delay line. The gate length and width for all the GaAs MESFETs are 1·5 μm and 300 μm, respectively. Silicon nitride capacitors are used between stages for DC blocking and microstrip lines are used for impedance matching. The chip size is 5 mm × 3·5 mm.

(GGG) substrate with 100 μm-thick yttrium-iron garnet (YIG) film is placed on top of the transducers. A 250 μm gap between the YIG film and the transducers is provided by alumina substrates supporting the GGG substrate. External chip capacitors are used for DC bypass but no bondwires or external components are needed in the microwave path.



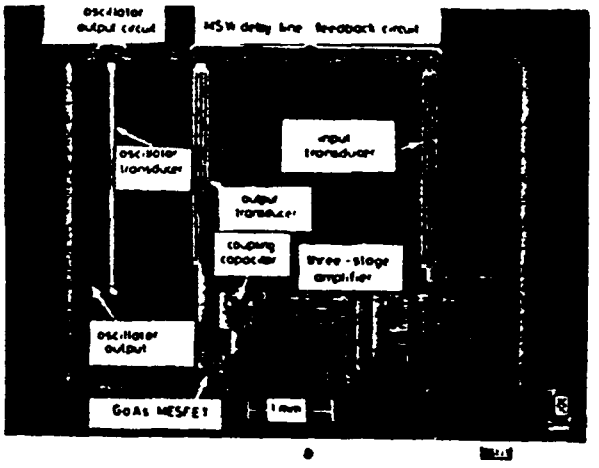


Fig. 1 *MSSW delay line oscillators using single GaAs chip*
a Schematic diagram of oscillator
b Photograph of GaAs MMIC chip

Experimental results: A magnetic field parallel to the YIG film and perpendicular to the direction of MSSW propagation is applied by an electromagnet. Fig. 2 shows the output of the oscillator, measured by a spectrum analyser. The oscillation frequency is 5·54 GHz with a magnetic field of 1244 G. The drain biases for the feedback and output amplifiers are 3·2 V and 2·6 V, respectively. The spectrum shows a very low phase noise, −100 dBc/Hz at 10 kHz offset, which compares favourably with YIG-sphere oscillators.[1] The oscillator maintains this low phase noise for the entire tuning range.

The oscillation has a single mode and the frequency can be tuned continuously from 4·82 GHz (1030 G) to 6·39 GHz

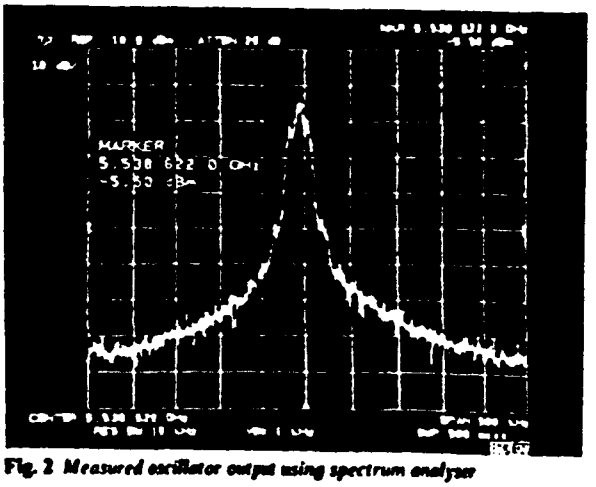


Fig. 2 *Measured oscillator output using spectrum analyser*
Oscillation frequency = 5·539 GHz, frequency span = 500 kHz

(1561 G). The oscillation frequency changes linearly with the applied magnetic field, at the rate of 2·96 MHz/G. No frequency jumping is observed for the entire 1·57 GHz tunable range because the monolithic integration of the feedback amplifier on a single GaAs chip, and the elimination of the directional coupler, give rise to extremely short external electrical delays. In contrast, all previously reported designs have used hybrid integration and external directional couplers. The frequency discontinuity for these oscillators can occur as frequently as every 120 MHz of tuning.[3] It appears that the upper oscillation frequency is limited by the lack of gain in the feedback amplifier. The maximum output power of the oscillator is 4·4 dBm at 6·1 GHz. The output power may be increased with proper matching circuits to the output MESFET.

When the DC biases described above are applied to the MESFETs, multiple-mode oscillation occurs at frequencies below 4·8 GHz. At these lower frequencies the feedback amplifier has higher gain and the MSSW delay line has wider passband.[4] Consequently, the phase and gain requirements for oscillation are satisfied at more than one frequency at any magnetic field. Although the higher-mode oscillations can be suppressed by reducing the gain of the feedback amplifier, the tunable frequency range is reduced as well. At a lower bias of 2·1 V, the lower gain of the amplifier results in single-mode oscillation that can be tuned continuously from 2·97 GHz (365 G) to 4·51 GHz (950 G), a tunable range of 1·54 GHz. The upper frequency can be increased from 4·51 GHz to 4·80 GHz with higher magnetic field if the DC bias is adjusted at each magnetic field to maintain a single-mode oscillation. When the magnetic field is further increased the circuit ceases to oscillate. However, the oscillation resumes at 4·826 GHz and single-mode oscillation can be maintained up to 6·39 GHz as described above.

Conclusion: We have, for the first time, developed a microwave tunable oscillator using only a single *YIG/GGG* MSSW delay line and a single GaAs MMIC chip. Because the output of the oscillator is taken directly from an amplifier on the GaAs chip, no directional coupler or external feedback circuit is needed. As a result, the size and external electrical delay of the oscillator are much smaller than any previously-reported oscillator using magnetostatic-wave delay lines. The oscillator has very wide tunable range and low phase noise. Single-mode oscillation can be achieved from 2·97 GHz to 6·39 GHz with only a small discontinuity at 4·8 GHz. The tunable frequency range is limited by the bandwidth of the feedback amplifier. This tunable oscillator may be operable above 20 GHz by using a wideband GaAs feedback amplifier.

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C. L. CHEN
L. J. MAHONEY
Lincoln Laboratory
Massachusetts Institute of Technology
Lexington, MA 02173, USA

19th December 1988

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NEURAL NETWORK CAPACITY USING DELTA RULE

Indexing terms: Neural networks, Memories, Networks, Associative memory, Content-addressable memory, Artificial intelligence, Capacity

It is shown that modifying the Hopfield neural network model to use the delta rule rather than the Hebbian rule substantially increases the capacity. The number of patterns one can store in a neural network of N neurons is actually greater than N (unless N is very small). For example, for $N = 30$, one can store 40 patterns with a success rate of close to 90%.

Introduction: Over the past several years, several papers have been published on the capacity of neural networks. Hopfield, in his landmark paper,[1] predicted experimentally that the number of patterns that one could store in a neural network of N neurons is approximately $0{\cdot}15N$. Others[2] have shown that the capacity of the Hopfield model is of the order of $N/\log N$ assuming that the Hebbian rule is used to determine the weight matrix T. The number of patterns one can store in a neural network can be greatly increased by using other learning algorithms such as the delta rule. Abu-Mostafa and St. Jacques[3] indicated that the number of arbitrary patterns that one can store in Hopfield network of N neurons is bounded above by N regardless of the method of obtaining the weight matrix. Their definition of capacity m is that every set of m patterns that one wishes to store has an associated zero-diagonal weight matrix T (and threshold vector t) such that each pattern is a fixed point. We show that, with the delta rule, the capacity is actually greater than N (except for small N). Our definition of capacity m is that one can almost always store m patterns in a neural network that does not allow direct self-feedback, and show how to recognise such sets of patterns.

Recognising sets of patterns that cannot be stored: We have previously shown that, if two patterns differ by only one bit, they cannot be stored simultaneously in a neural network that does not allow direct self-feedback.[4] Let the calculation of the next state of neuron i be as follows:

$$x_i = \sum_{j \neq i} T_{ij} V_j \tag{1}$$

$$V_i = \begin{cases} 1 & x_i > 0 \\ -1 & x_i \leq 0 \end{cases} \tag{2}$$

If two patterns differ in the ith bit only, the calculation of x_i will be identical regardless of which of those two patterns is applied to the network. If one of the two patterns is a stable state, the other will have as a next state that same stable state. By a similar argument, if two patterns differ in $N - 1$ bits, they cannot (usually) be stored simultaneously. In this case, let bit i be the only bit in which the two patterns match. If application of one pattern to the net produces x'_i, application of the other pattern will produce $-x'_i$. Only if $x'_i = 0$ can both patterns be stored simultaneously. Note that, as N increases, the likelihood that two patterns differ by 1 or by $N - 1$ bits decreases exponentially.

Since, for any neural network with zero-diagonal weight matrix, there exists pairs of patterns that cannot be stored simultaneously, the definition of capacity used by Abu-Mostafa and St. Jacques must be revised. We can only speak in terms of storing randomly chosen patterns with a certain probability.

Tests: Several tests were run to estimate experimentally the capacity of the neural network model described by eqns. 1 and 2 using the delta rule

APPENDIX B

Oscillators Using Magnetostatic-Wave Active Tapped Delay Lines

C.L. Chen, A. Chu, L.J. Mahoney, W.E. Courtney, R.A. Murphy, and J.C. Sethares

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This paper is another example of the hybrid integration of a microwave GaAs circuit with a YIG delay line tapped at five different points. The circuit forms an oscillator with an extremely short external delay loop and the taps provide multiple outputs with long time delays. The oscillator is tunable from 2.76 to 2.95 GHz with a 3-dB bandwidth of 10 kHz.

Oscillators Using Magnetostatic-Wave Active Tapped Delay Lines

CHANG-LEE CHEN, MEMBER, IEEE, ALEJANDRO CHU, LEONARD J. MAHONEY, WILLIAM E. COURTNEY, SENIOR MEMBER, IEEE, R. ALLEN MURPHY, MEMBER, IEEE, AND JAMES C. SETHARES, SENIOR MEMBER, IEEE

Abstract — A novel oscillator that combines a magnetostatic wave (MSW) tapped delay line with GaAs monolithic microwave integrated circuits (MMIC's) has been fabricated. This oscillator incorporates an external feedback loop which is extremely short and provides multiple outputs delayed in time by the MSW delay line. The oscillator is tunable from 2.76 to 2.95 GHz and the 3-dB bandwidth of the oscillation is approximately 10 kHz.

I. Introduction

DEVICES based on the propagation of magnetostatic waves (MSW's) have the potential of performing signal processing at microwave frequencies, a frequency range where surface acoustic wave devices do not operate [1]. MSW delay lines provide useful time delays up to approximately 20 GHz, and because they are planar they can be integrated with other components, such as GaAs monolithic microwave integrated circuits (MMIC's). In particular, a tunable oscillator using MSW delay lines is attractive because of its simple structure, superior phase-noise characteristics [2], and large tunable bandwidth. Tunable oscillators using MSW delay lines, external amplifiers, and directional couplers have been reported [3], [4]. However, undesirable frequency jumping was observed within the frequency tuning range because of the electrical length of the feedback loop.

We have developed a novel tunable oscillator that integrates MESFET amplifiers and MSW transducers on a single GaAs chip. An active tapped delay line was realized using five GaAs MMIC chips and one gallium gadolinium garnet (GGG) substrate with an epitaxially grown yttrium ion garnet (YIG) film to support MSW propagation. An oscillator was formed by coupling the signal from the first tap to the input amplifier of the delay line. The additional delay-line taps provide time-delayed outputs of the oscillator. Because monolithic-circuit chips were used and no directional coupler is required, the oscillator is compact and the feedback loop is short. The time delay of the multiple outputs is determined by the spacing between taps and by the applied magnetic field. In this work we present a new approach to the fabrication of a tunable MSW oscillator and also demonstrate the feasibility of integrating MSW devices with GaAs MMIC's.

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C. L. Chen, L. J. Mahoney, W. E. Courtney, and R. A. Murphy are with the Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, MA 02173.

A. Chu was with the Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, MA 02173. He is now with M/A-COM, Inc., Burlington, MA 01803.

J. C. Sethares is with the Rome Air Development Center, Hanscom Air Force Base, MA 01731.

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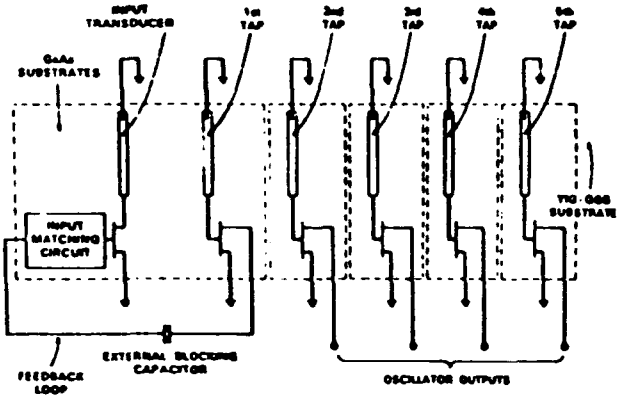

Fig. 1. Schematic diagram of the oscillator using an active tapped delay line.

II. Oscillator Design and Fabrication

The schematic diagram of the oscillator is shown in Fig. 1. The active tapped delay line was constructed using an input GaAs chip incorporating the input amplifier and output circuitry for the feedback tap (tap 1) and four other GaAs chips incorporating only the output circuitry for the oscillator outputs (taps 2–5). The circuit diagram and a photograph of the completed GaAs MMIC chip are shown in Fig. 2(a) and (b), respectively. The design and fabrication of the input amplifier have been previously reported [5]. The input circuitry consists of a 500-μm-wide MESFET (FET 3) with a distributed matching network connected to its gate and the input MSW transducer connected to its drain. This circuit provides convenient impedance matching to the MSW delay line and produces amplification of the input signal. The output transducer of the delay line is connected to the gate of FET 1 and gain modulation is provided by a shunting MESFET (FET 2), which is used as a variable resistor. The spacing between

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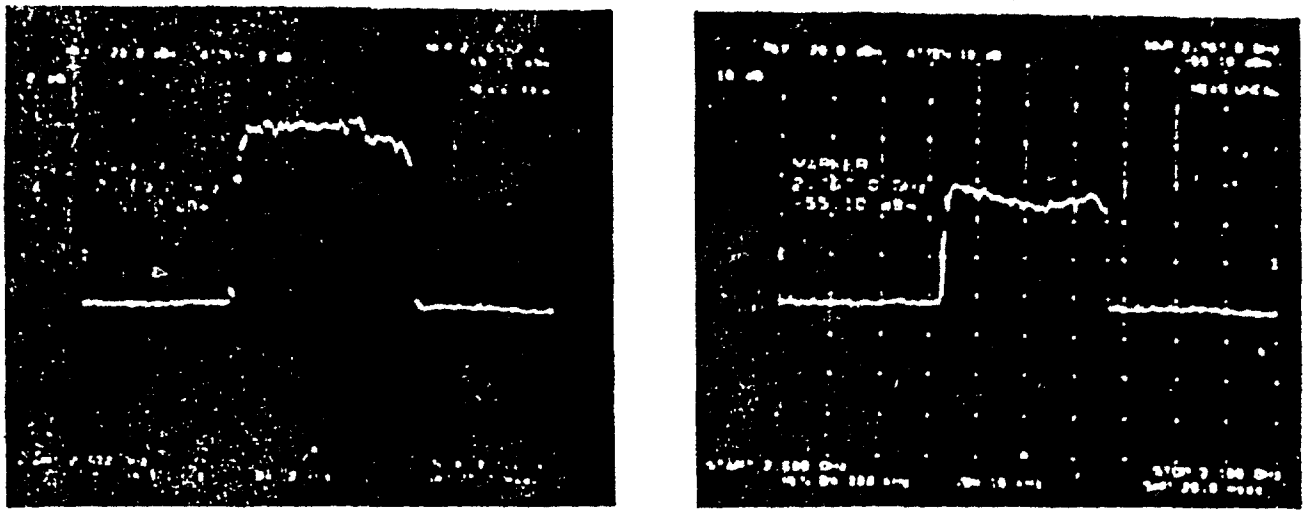

(a) (b)

Fig. 5. Measured tunable range of the oscillator using a spectrum analyzer. A maximum hold feature, which stores the greatest signal measured at each frequency as the magnetic field is increased, is used to show the oscillation frequency range. (a) Tap 2. (b) Tap 4.

III. Experimental Results

The output gain at each tap of the delay line can be varied by changing the drain source resistance of FET 2 or the bias applied to the drain of FET 1. When a signal was applied to the input amplifier with the feedback loop disconnected, a maximum gain of 3.5 dB was measured at the first tap of the delay line at 2.5 GHz. The measurement was performed with 200 G of applied magnetic field. Therefore, GaAs MESFET's provided the net gain needed to sustain the oscillation. More than 12 dB of gain variation was achieved by changing the drain bias of FET 1 from 3 to 0.2 V. At the same frequency an average time delay of 7.8 ns between each tap was measured, and as expected, did not change with the bias applied to the drain of the output FET.

Because all the components are assembled inside a small package and no directional coupler is used, the electrical length of the feedback loop is extremely short. From measured amplifier data, this external electrical delay is estimated to be 0.1 ns, which is approximately 1 percent of the total time delay of the MSW delay line. For comparison, the external delay was approximately between 10 and 20 percent of the total time delay in a previously reported work [4] in which an external amplifier and a directional coupler were used.

The outputs of the oscillator were obtained from taps 2 through 5. The phase difference between these outputs is determined by the propagation delay of the MSW between the taps. Fig 4 shows the oscillator output taken from tap 2. Two oscillation modes are observed, separated by approximately 100 MHz. These two modes exist because the single-line wide-band transducers which were used do not provide adequate frequency discrimination. The measured output power of the oscillation at 2.78 GHz is -42.1 dBm and the 3-dB bandwidth is approximately 10 kHz, demonstrating that this is a high-Q oscillator. The frequency of the oscillator can be tuned continuously from 2.76 to 2.95 GHz by changing the applied magnetic field from 210 to 280 G. No frequency jumping was observed and we believe that this oscillator can operate over a much wider frequency range without frequency jumping because of the short length of the external circuit. The current tuning range of 190 MHz was limited by the gain and bandwidth of the amplifiers in the feedback circuit. By reducing the gain from the first tap, the second oscillation can be suppressed and a single-mode oscillator can be created at the expense of a smaller tunable range.

Spectrum analyzer displays in Fig. 5(a) and (b) show the measured outputs from taps 2 and 4, respectively, as the magnetic field varies from 210 to 280 G. Notice that the tunable range of the two taps is nearly identical, while the average output power from tap 4 is approximately 14 dB lower than that from tap 2. This attenuation is estimated to arise from the nonuniformity of the magnetic field (~ 8 dB), the power coupled to tap 3 which lies between taps 2 and 4 (~ 2 dB), and the propagation loss of the 4-mm-long MSW delay line between taps 2 and 4 (~ 4 dB).

IV. Conclusions

We have, for the first time, fabricated a GaAs MMIC designed specifically for use with MSW devices and demonstrated that the performance of MSW devices can be greatly improved by integrating them with GaAs MMIC's. This new combination of MSW devices and GaAs MMIC's has been used to construct a five-tap MSW active delay line and to realize a novel MSW delay-line oscillator by feeding the signal from the first tap back to the input amplifier. This provides a high-Q tunable oscillator with multiple outputs having a built-in time delay. This unique property of the oscillator may be very useful in phased array technology [1]. Because of the use of GaAs

James C. Sethares (M'65–SM'82) was born in Hyannis, MA, in 1928. He received the B.S. degree in electrical engineering from the University of Massachusetts in 1959, and the M.S. degree in electrical engineering from Massachusetts Institute of Technology, Cambridge, in 1962.

He then joined the Microwave Physics Laboratory of Air Force Cambridge Research Laboratories, Hanscom Air Force Base, Bedford, MA, where he is now employed as a Research Physicist in the Electromagnetic Sciences Directorate of Rome Air Development Center. For many years, he was a Visiting Lecturer in mathematics at Boston University and a Visiting Lecturer in electromagnetics at the University of Lowell. In the past, he has worked on dielectric resonators, acoustic waves for nondestructive evaluation, and cholesteric liquid crystals for microwave and millimeter-wave power pattern visualization. More recently, his main area of interest is microwave magnetics including magnetostatic wave technology.

APPENDIX C

Molecular Beam Epitaxial Growth of GaAs on Gadolinium-Gallium Garnet

A.R. Calawa and M.J. Manfra, Journal of Electronic Materials **19**, 975 (1990)

This paper describes the first successful growth of single-crystal GaAs on GGG. It also represents the first time that any electrical measurements are reported in the growth of any III-V compound semiconductor on a garnet substrate.

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Molecular Beam Epitaxial Growth of GaAs on Gadolinium-Gallium Garnet

A. R. CALAWA and M. J. MANFRA

Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, MA 02173-9108

Single-crystal GaAs has been grown by molecular beam epitaxy on $Gd_3Ga_5O_{12}$ (GGG) using an InAs buffer layer and an InAs/GaAs multilayer structure between the GGG and the GaAs. The x-ray diffraction spectrum shows that both the InAs and GaAs epitaxial layers are oriented in the (111) direction when grown on a (100) GGG substrate. The unintentionally doped InAs layers are *n*-type and have donor concentrations in the range of 7×10^{16} to 2×10^{18} cm^{-3} which vary inversely with growth temperature. The corresponding carrier mobilities vary from 3.5×10^3 to 1×10^5 cm^2/V s. The GaAs was also found to be conducting. The 77-K photoluminescence (PL) spectrum of the GaAs grown on the GGG differs from that of homoepitaxial GaAs in that the heteroepitaxial GaAs PL intensity is approximately 50 times lower, its linewidth is five times broader, and its peak energy is blue shifted by 10 meV.

Key words: Gadolinium gallium garnet, GGG, GaAs, molecular beam epitaxy, InAs

1. INTRODUCTION

Over the past decade there has been considerable interest in devices using ferrimagnetic garnets. Of particular interest are microwave non-reciprocal devices such as circulators and isolators, and devices based on the propagation of a magnetostatic wave (MSW) in films of these materials. Circulators, which are used to isolate different parts of an electromagnetic circuit, are the most employed microwave component. Ferrimagnetic garnet circulators which have operated at frequencies up to 22 GHz have low insertion losses (<0.5 dB) and bandwidths as large as one octave.[1] Also, several MSW components such as delay lines, filters, resonators, correlators and convolvers have been realized and used for analog signal identification, control and processing.[2] These components enable a substantial reduction in the device size required for long delays because MSWs travel with velocities two to four orders of magnitude slower than electromagnetic waves. In addition, they can operate in microwave frequency bands (0.5–26.5 GHz) with bandwidths as large as 1 GHz and have a planar geometry that is compatible with monolithic microwave integrated circuits (MMICs).

Because of its low propagation loss, the most frequently used ferrimagnetic film is yttrium-iron garnet (YIG) grown by liquid phase epitaxy on a gadolinium-gallium garnet (GGG) substrate.[3] The GGG substrate is particularly desirable because YIG films that are lattice matched and essentially defect free (<1 cm^{-2}) can be grown on large diameter (>3 in.) GGG wafers. The integration of magnetic microwave non-reciprocal devices and of MSW devices with MMICs is currently a hybrid technique. One method used in this integration involves gluing or soldering the circuit chips and the YIG devices together in order to make the wire interconnects. This is a cumbersome process with a low yield, and the interconnect wires can limit the circuit performance. Clearly, a need exists for the monolithic integration of semiconductor microwave devices with the non-reciprocal and the MSW devices. In this paper, we report on the molecular beam epitaxy (MBE) of GaAs on GGG, the first step in such an integration.

To our knowledge there have been only two reports of the epitaxial growth of III-V compounds on a garnet and both utilized organometallic vapor phase epitaxy. In one case[4] an InP layer that contained several GaInAs quantum wells was grown on GGG. The lattice-constant mismatch between the InP and GGG was 52.6%. In the second case[5] a GaAs film was grown on a garnet in which the rare-earth composition was adjusted to obtain lattice sites that were more nearly coincident with the GaAs lattice sites. The mismatch was 52.7%. The electrical characterization of the layers was not reported in either case.

2. EXPERIMENT

The chemical composition of GGG is $Gd_3Ga_5O_{12}$, and the basic crystal structure is cubic with a lattice parameter of 12.383Å. The basic crystal structure of GaAs is also cubic, but the lattice parameter is only 5.653Å. The lattice-constant mismatch between the two structures is 53.4%. Even if the GaAs were to be grown such that every second site were coincident with a GGG site, the mismatch would be 8.7%. In spite of this large mismatch, attempts were made to grow GaAs directly on (100) GGG by MBE at a substrate temperature of 580° C. *In situ* reflection high-energy electron diffraction (RHEED) patterns indicated that the resulting thin films (<2,000Å) were crystalline; the films became polycrystalline when thicker layers were grown. The thin crystalline films were always highly insulating and could easily be etched from the GGG substrate with hydrofluoric acid. We concluded that the films were

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Table I. Comparison of the Calculated and Experimental Values of 2θ X-ray Diffraction Peaks for InAs and GaAs Layers Grown on GGG

Layer	Crystal Orientation (hkl)	2θ Calculated (Deg)	2θ Experimental (Deg)
InAs	(111)	25.44	25.42
InAs	(222)	52.26	52.20
GaAs	(111)	27.31	27.30
GGG	(400)	28.83	28.83
GGG	(800)	59.73	59.68

layer orientation than near neighbor lattice-site coincidence.

Nomarski and scanning electron micrographs of the GaAs surface on the structure of Fig. 1 are shown in Figs. 3a and 3b, respectively. The rough surface morphology observed in the photographs indicates that the growth is primarily three dimensional and proceeds by the formation of islands that coalesce as the layer thickness increases. The island growth is also manifested in the RHEED pattern as rows of bright spots instead of the lines observed from smooth surfaces. The island coalescence is verified by electrical-conduction continuity as discussed below.

Van der Pauw measurements were made on several films at different stages of the layer growth.

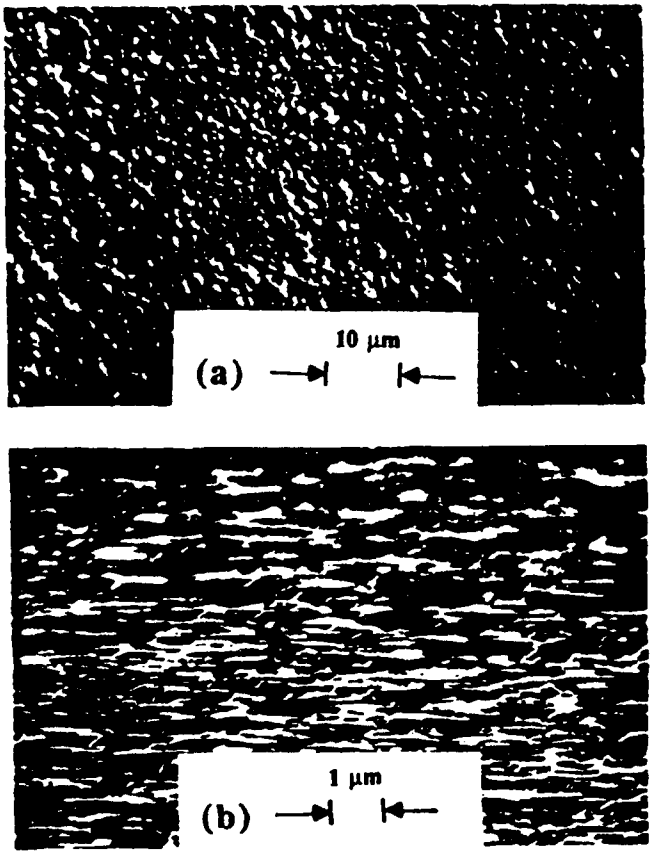

Fig. 3 — Micrographs from (a) Nomarski and (b) scanning electron microscope studies of the GaAs surface on the layer structure of Fig. 1.

Figure 4 is an Arrhenius plot of the carrier concentration and mobility of several unintentionally doped ~1-μm-thick InAs layers grown on GGG at different substrate temperatures. The carrier concentration of the layers was found to vary exponentially with the inverse of the growth temperature. This phenomenon is probably due to a volatile impurity coming from one of the sources.[8] As the substrate temperature increases, the sticking coefficient of the impurity decreases, resulting in a lower carrier concentration. The activation energy for this process, as obtained from the plot of Fig. 4, is 0.073 eV. The carrier mobility, also shown in Fig. 4, varies inversely with carrier concentration, as expected. These values are about 10% of those obtained in high-quality InAs with the same concentration, but they are believed to be quite reasonable for these heteroepitaxial layers considering the strain and high defect density usually associated with lattice-mismatched heteroepitaxy. Van der Pauw measurements were also made on the structure shown in Fig. 1, even though parallel conduction occurs in each of the layers and in the InAs quantum wells. If the entire structure is treated as one layer, a concentration of 6×10^{17} cm^{-3} donors is obtained with a mobility of 1500 cm^2/V s. These numbers are difficult to interpret because of the complexity of the structure and the poor morphology of the layers, but they do indicate that the GaAs is conducting. To our knowledge these are the first electrical measurements ever made on a semiconductor grown on a garnet.

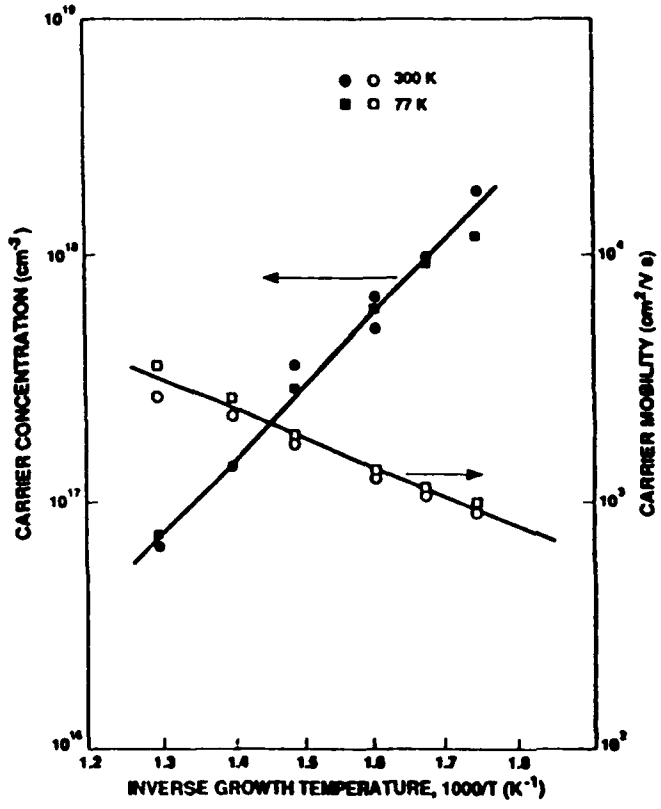

Fig. 4 — Arrhenius plot of InAs donor concentration and carrier mobility as a function of inverse growth temperature.

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